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Robert J. Depke

Inventor: Hiroyuki Ikeda
For: Thin Film Transistor Apparatus
Serial No.: 09/821,636
Art Unit: 2811
Filed: March 29, 2001
Attorney Ref.: 075834.00064

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Filing Date	March 29, 2001
First Named Inventor	Hiroyuki Ikeda
Art Unit	2811
Examiner Name	Thien F. Tran
Attorney Docket Number	075834.00064

ENCLOSURES *(Check all that apply)*

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- ☐ Fee Attached
- ☑ Amendment/Reply
- ☑ After Final
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Response to Non-Conforming Appeal Brief

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.:	09/821,636	**Confirmation No.:**	5712
Applicant:	Hiroyuki Ikeda		
Filed:	March 29, 2001		
TC/A.U.:	2811		
Examiner:	Thien F. Tran		
Docket No.:	075834.00064		
Customer No.:	33448		

APPEAL BRIEF IN RESPONSE TO NOTICE OF NON-COMPLIANCE

In response to the Notification of Non-Compliant Appeal Brief mailed on August 1, 2006, Applicants submit herewith an amended copy of the brief which sets forth a more detailed cross reference between the claim language of independent claims 1 and 39, and the drawings and specification. Applicants have also added an Evidence Appendix and Claims Appendix in which they more clearly set forth that no such Appendix is required. Applicants submit that, in light of the foregoing, this Appeal Brief meets all of the requirements of 37 C.F.R. §41.37, and request that the Appeal be forwarded to the Examiner to prepare an Answer.

I. REAL PARTY IN INTEREST

The real party in interest is Sony Corporation as a result of transfer of all right, title and interest to the subject matter of this Application Serial No. 10/466,661, via the Assignment recorded in the Patent Office in Reel 011664 Frame 0777 on March 29, 2001.

II. RELATED APPEALS AND INTERFERENCES

Applicants note that this case was first submitted to a Pre-Appeal Brief Request for Review on April 3, 2006. A decision was mailed on May 12, 2006. Applicants and the undersigned are unaware of any further related judicial proceedings, appeals, or interferences in relation to the instant Appeal.

III. STATUS OF CLAIMS

The claims currently stand in condition as modified by the Response to Restriction on July 8, 2002, as further modified by the Amendment of December 26, 2002 amending claims 1 and 2 and canceling claims 4 and 5, as further modified by the Amendment of February 17, 2005, amending claim 1 and adding new claim 39, and as finally modified by the Amendment of August 12, 2005 amending claims 1, 2, and 39 and adding new claims 40 and 41. Accordingly, claims 1 – 3 and 39 – 41 are currently rejected and appealed, and stand in condition as set forth in the attached Appendix of Claims on Appeal.

IV. STATUS OF AMENDMENTS

No Amendment After Final effecting the claims has been filed or entered by the Examiner. Accordingly, all remaining claims stand in the same condition as they did at the time of the November 02, 2005 Final Office Action.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention relates to a thin-film semiconductor apparatus employed for driving a liquid crystal display, and a method for driving the same. More particularly, the present invention is concerned with a technique for controlling threshold voltages for thin-film transistors integrated in a thin-film semiconductor apparatus.

As noted in the specification at page 1, beginning at line 17, when thin-film transistors are integrated in a thin-film semiconductor apparatus such as a liquid crystal display, amorphous silicon or polycrystalline silicon is used as an active layer. The specification also notes that certain problems are encountered in using thin-film semiconductor transistors for a liquid crystal display. For example, the threshold voltage of the transistor may be varied and is likely to change with time. See, for example, Applicant's specification at page 3 lines 15-30. Furthermore, when using polycrystalline silicon for thin-film transistors that is obtained by crystallizing amorphous silicon through the use of the laser annealing method or the like, the crystalline characteristics may be varied due to fluctuations in the radiation conditions for the laser beam. The result is that the threshold may be varied in the range of from about one to 2 V. See, applicant's specification at page 4 in lines 1-10. Obviously, the variations in threshold voltage for the thin-film transistors of a liquid crystal display can have serious deleterious effects which adversely impact the visual characteristics of the display.

Additionally, Figure 5B shows an example of the prior art problem of leakage current flowing through transistors N1 and N2, of which the present invention is directed to curing. More specifically, as noted on pages 3 - 5 of the specification, when forming a circuit as shown in Fig. 5B on an insulating substrate such as glass, the threshold voltage may be varied and is likely to be changed with time. Furthermore, the structure of the polycrystalline silicon obtained by laser annealing of the orifice a silicon causes fluctuations in the mobility

of carriers within the film, which also causes variations in the threshold voltage of the device. Because of these variations, prior art devices have exhibited the disadvantageous phenomenon that although the thin-film transistor should be in an off state, it is in an on state due to the dispersion of these properties, causing the circuit to erroneously operate. (See page 4 of the Specification).

Applicant's present invention overcomes the problems and deficiencies inherent in the prior art by providing a novel approach to overcoming the problems associated with the recognized threshold voltage fluctuations.

As noted in independent claim 1, a display apparatus according to the present invention includes (See Figures 1 and 8) a plurality of thin film transistors TFT, each of the thin-film transistors comprising a thin-film constituting a channel 'Ch' and having a threshold voltage, a first gate electrode 2F on one side of the channel, and a second gate electrode on an opposite side of the channel 2R, and further comprising a means (said means comprising an opposing gate electrode 2R and an attached signal line for applying a voltage to the opposing gate electrode as shown in Figures 1 and 8) for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode 2R when the first gate electrode 2F receives a first control voltage (See Figure 5A and pages 24 – 25 of the disclosure, wherein the threshold adjustment voltage applied to the second gate electrode of transistor N1 is -5V during non-selection time, at which time a signal of 0V is applied to the first gate electrode of N1) and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode 2R when the first electrode 2F receives a second control voltage (See Figure 5A and pages 24 – 25 of the disclosure, wherein the threshold adjustment voltage applied to the second gate electrode of transistor N1

is +10V during selection time, at which time a signal of +10V is applied to the first gate electrode of N1). See also, page 15, lines 14 – 30 of the disclosure.

As noted in independent claim 39, a display apparatus according to the present invention includes (See Figures 1 and 8) a plurality of thin film transistors TFT, each of the thin-film transistors comprising a thin-film constituting a channel 'Ch' and having a threshold voltage, a first gate electrode (2R in Fig. 1, 2F in Fig. 8) above said semiconductor thin film, and a second gate electrode (2F in Fig. 1, 2R in Fig. 8) below said semiconductor thin film, and further comprising a means (said means comprising an opposing gate electrode 2R and an attached signal line for applying a voltage to the opposing gate electrode as shown in Figures 1 and 8) for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode 2R when the first gate electrode 2F receives a first control voltage (See Figure 5A and pages 24 – 25 of the disclosure, wherein the threshold adjustment voltage applied to the second gate electrode of transistor N1 is -5V during non-selection time, at which time a signal of 0V is applied to the first gate electrode of N1) and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode 2R when the first electrode 2F receives a second control voltage (See Figure 5A and pages 24 – 25 of the disclosure, wherein the threshold adjustment voltage applied to the second gate electrode of transistor N1 is +10V during selection time, at which time a signal of +10V is applied to the first gate electrode of N1). See also, page 15, lines 14 – 30 of the disclosure.

As noted in claims 1 and 39, the current invention applies different threshold voltages to the rear gate electrode corresponding to whether the transistor is in the on state (a first control voltage being applied to the control gate) or in the off state (a second control voltage

being applied to the control gate). As discussed on page 8 of the specification, by actively controlling the threshold voltage during off operation of the transistor, the current flowing through the channel when the transistor is in the off state advantageously decreases compared to the prior art devices. Furthermore, by actively controlling the threshold voltage during on operation of the transistor, the current flowing through the channel during on operation can be advantageously increased compared to the prior art devices. (See page 8 of the specification).

As noted in dependent claims 40 and 41, a display apparatus according to the present invention further includes (See Figures 1, 7, and 8) the limitation wherein the voltage applied to the first gate electrode 2F is different from the threshold adjustment voltage applied to the second gate electrode 2R during voltage application / transistor selection. (See Figure 7 and page 26 of the disclosure, wherein the threshold adjustment voltage applied to the second gate electrode of transistor N1 is +5V during selection time, at which time a signal of +10V is applied to the first gate electrode of N1). See also, page 26, lines 20 - 28 of the disclosure.

The prior art fails to teach or suggest such a device.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Whether the teachings of the *Kubota* (U.S. Patent No. 5,808,595) reference provides the requisite disclosure in order to render anticipated claims 1 – 3 and 39 - 41 under 35 U.S.C. §102(b), or in the alternative, render the claimed invention obvious under 35 U.S.C. §103(a).

VII. ARGUMENT

Applicant respectfully submits that the prior art reference of record, whether considered alone, or in combination, fails to anticipate, teach, or suggest Applicant's presently claimed invention. As detailed below, the rejection set forth by the Examiner is improper.

A. **The Cited Reference Fails to Anticipate the Claimed Invention as specified in Claims 1 – 3, and 39 - 41.**

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3, and 39 - 41 under 35 U.S.C. §102(b). Examiner has rejected these claims in view of the cited prior art reference of *Kubota* (U.S. Patent No. 5,808,595).

Claim 1 currently contains the following limitations, numerically numbered for ease of reference:

> 1) A display apparatus comprising: a plurality of thin film transistors, each of said thin film transistor comprising a semiconductor thin film constituting a channel and having a threshold voltage, and a first gate electrode on one side of said semiconductor thin film and a second gate electrode on an opposite side of said semiconductor thin film,
>
> 2) and further comprising a means for adjusting the threshold voltage by
>
> 3) applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and
>
> 4) applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode when the first electrode receives a second control voltage.

Independent claim 39 contains similar claim limitations.

Applicants note that the Court of Appeals for the Federal Circuit has held that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Applicants submit that the *Kubota* reference fails to anticipate each and every element of the currently claimed invention.

Regarding claims 1 and 39, Applicants submit that the prior art reference cited by the examiner fails to teach or suggest the application of two different threshold adjustment voltages to a rear gate electrode depending on the current state of the transistor. More specifically, each of claims 1 and 39 require that a first threshold adjustment voltage be applied to the rear gate electrode when the front gate electrode receives a first control voltage, and a second threshold adjustment voltage be applied to the rear gate electrode when the front gate electrode receives a second control voltage.

As noted in the Summary of the Invention section above, the current invention applies different threshold voltages to the rear gate electrode corresponding to whether the transistor is in the on state (a first control voltage being applied to the control gate) or in the off state (a second control voltage being applied to the control gate). As discussed on page 8 of the specification, by actively controlling the threshold voltage during off operation of the transistor, the current flowing through the channel when the transistor is in the off state advantageously decreases compared to the prior art devices. Furthermore, by actively controlling the threshold voltage during on operation of the transistor, the current flowing

through the channel during on operation can be advantageously increased compared to the prior art devices.

Importantly, in order to recognize both of these advantages, the threshold adjustment voltage applied to the rear Vth gate must be adjustable during circuit operation, and must be adjusted corresponding to the application of either a first control voltage or a second control voltage being applied to the front control gate.

While the *Kubota* reference does suggest that the threshold voltage adjustment applied to a rear gate can be varied in order to adjust the threshold voltage of a control gate, it does not teach or suggest changing the applied voltage during circuit operation, nor does it teach or suggest varying the applied voltage based upon the respective application of a first control voltage or a second control voltage to the control gate of the transistor.

The Kubota reference, rather, actually teaches away from varying the Vth adjustment voltage applied to the rear gate. See, for example, Column 12, lines 30 – 31, which clearly states that the voltage applied to the conductive electrode 14 is constant. In other words, it does not change based upon the application of one of two or more voltages applied to the front gate.

The Examiner, on page 3 of the November 2, 2005 Office Action, stated that "it is obvious that the voltage Vgs [of the Kubota reference] applied to the first gate electrode varies during the operation (0V with a transistor is not selected, off state or -4V to 8V when the transistor is selected) is different from the threshold adjustment voltage (-20V as solid line shown in Fig. 4) applied to the second gate electrode during voltage application."

The Examiner, on page 2 of the November 2, 2005 Office Action, also cites to Column 13, lines 27 – 38 as teaching the application of two different Vth adjustment voltages

to the second gate electrode (the conductive electrode 14). This portion of the reference states that "In this graph, the characteristic that is obtained when no bias voltage is applied to the conductive electrode ... is indicated by a broken line, and the characteristic that is obtained when a bias voltage of -20V is applied to the conductive electrode is indicated by a solid line. These characteristics show that the threshold voltage is shifted by 2.5V by the application of the bias voltage to the conductive electrode." (Column 13, lines 30 – 38)

However, nothing in this cited portion supports the Examiner's position that the reference teaches the limiatation of claims 1 and 39 requiring the application of two different Vth adjustment voltages during circuit operation and based upon what voltage is applied to the control gate.

Rather, Applicants submit that Figure 4 and Column 13, lines 27 – 38 are consistent with the statement in Column 12, lines 30 – 31 of the reference that constant voltages are applied to the conductive electrode 14. More specifically, as shown in Fig. 4, a Vth adjustment voltage of 0V or -20V is applied throughout the entire range of control voltage application. More specifically, neither Figure 4 nor Column 13, lines 27 – 38 teaches changing the Vth adjustment voltage based on the applied control voltage. Applicants submit that Figure 4 would not show two distinct lines (one solid, one dotted) if it taught the application of one Vth adjustment amount when a first control voltage is applied, and a second different Vth adjustment amount when a second control voltage is applied. Rather, if *Kubota* were to actually teach Applicant's currently claimed invention, there would only be one line shown in Figure 4, and it would transition from a dotted line (signifying the application of a first Vth adjustment amount when a first control voltage is applied) to a solid line (signifying the application of a second different Vth adjustment amount when a second

control voltage is applied). In contrast to this, Figure 4 shows two distinct lines, signifying the application of two constant Vth adjustment values (0V or -20V) during the entire range of circuit operation and control gate voltages (-4V to 8V). Only one of these values (0V or -20V) is applied, based upon the desired Vth value for operation of the circuit, and that value never changes during circuit operation.

In summary, Applicants submit that the Examiner has failed to assert a prima facie case of anticipation, and that in fact, the *Kubota* reference actually teaches away from Applicant's currently claimed invention by teaching the application of a constant voltage during circuit operation and throughout the range of control voltages applied to the opposing gate electrode. More specifically, *Kubota* fails to teach the variation of an applied voltage threshold adjustment amount, applied to one gate of the dual-gate structure, based upon what control voltage is being applied to the second gate of the dual-gate structure, and during normal circuit operation. Claims 1 and 39 require such operation in the language "means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode when the first electrode receives a second control voltage." Because *Kubota* fails to anticipate this limitation, Applicants submit that the rejection must be withdrawn in light of the *Verdegaal Bros. v. Union Oil Co. of California* precedent discussed above. Because each of the dependent claims 2 – 3 and 40 – 41 include all of the limitations of the base claim, Applicants submit that these claims are also not anticipated by the *Kubota* reference.

In specific regard to claims 40 and 41, Applicants submit that the Examiner has furthermore failed to identify a prior art reference which teaches that the voltages applied to the first and second opposing gate electrodes 2R and 2F during voltage application / transistor selection are different. For this reason also, Applicants submit that claims 40 and 41 are allowable over the prior art of record.

Accordingly, Applicants submit that claims 1 – 3 and 39 - 41 are allowable over the cited prior art, and respectfully request that the rejection be over-turned on appeal, and the remaining claims placed in condition for allowance.

B. **The Cited Reference Fails to Teach or Suggest the Claimed Invention as specified in Claims 1 – 3, and 39 - 41.**

Applicants respectfully request reconsideration of the Examiner's rejection of claims 1 – 3 and 39 – 41 under 35 U.S.C. §103(a). Examiner has rejected these claims in view of the cited prior art reference of *Kubota et al.* (U.S. Patent No. 5,808,595).

Under § 2143 of the MPEP, in order to establish a prima facie case of obviousness, the Examiner must meet three basic criteria. "First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." *MPEP §2143 rev. 3* (August, 2005). Applicants' assert that the Examiner has failed to establish a prima facie case of obviousness for at least the reason that the prior art reference fails to teach or suggest all of the claim limitations. Neither the primary reference nor any secondary

reference provides any indication that a second threshold adjustment voltage that is different than a first threshold adjustment voltage be applied depending upon the application of an alternate control voltage.

As discussed above, *Kubota* fails to teach or suggest the application of a second threshold adjustment voltage different than a first threshold adjustment voltage during circuit operation and based upon which of at least two control voltages are applied to the control electrode. Furthermore, the Examiner has failed to identify any other reference or source which even remotely provides the requisite suggestion to modify the cited primary reference for the purpose of resulting in the presently claim subject matter. There is simply no teaching her suggestion whatsoever which provides the appropriate support for the Examiner's alternate determination that the claimed invention is obvious in light of the prior art.

In light of the foregoing, Applicants submit that 35 U.S.C. §103 rejection must be withdrawn, and all remaining claims placed in condition for allowance.

CONCLUSION

In light of the foregoing, Applicant submits that the rejections of all claims are improper for the reasons noted and the rejections should all therefore be withdrawn.

Respectfully submitted,

Date: September 1, 2006

(Reg. #37,607)

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VIII. CLAIMS APPENDIX:

This listing of claims reflects the current status of the claims as they stand in light of the November 2, 2005 Final Office Action:

1. (Rejected) A display apparatus comprising:

a plurality of thin film transistors, each of said thin film transistor comprising a semiconductor thin film constituting a channel and having a threshold voltage, and a first gate electrode on one side of said semiconductor thin film and a second gate electrode on an opposite side of said semiconductor thin film,

and further comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage different than the first threshold adjustment voltage to the second gate electrode when the first electrode receives a second control voltage.

2. (Rejected) The semiconductor apparatus according to claim 1, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon which does not contain an impurity affecting the formation of a depletion layer, and has a thickness of 100 nm or less.

3. (Rejected) The semiconductor apparatus according to claim 1, wherein said semiconductor thin film constituting said channel is comprised of polycrystalline silicon

which contains an impurity effectively affecting the formation of a depletion layer, and has a thickness two times or less the maximum of the thickness of said depletion layer.

Claims 4-38 (Canceled).

39. (Rejected) A display apparatus comprising:

a plurality of thin film transistors, each of said thin film transistor comprising a semiconductor thin film constituting a channel and having a threshold voltage, and a first gate electrode above said semiconductor thin film and a second gate electrode below said semiconductor thin film,

and further comprising a means for adjusting the threshold voltage by applying a first threshold adjustment voltage to the second gate electrode when the first gate electrode receives a first control voltage and applying a second threshold adjustment voltage, different than the first threshold adjustment voltage, to the second gate electrode when the first electrode receives a second control voltage.

40. (Rejected) A display apparatus according to claim 1, further wherein the voltage applied to the first gate electrode is different from the threshold adjustment voltage applied to the second gate electrode during voltage application.

41. (Rejected) A display apparatus according to claim 39, further wherein the voltage applied to the first gate electrode is different from the threshold adjustment voltage applied to the second gate electrode during voltage application.

IX. EVIDENCE APPENDIX:

None.

X. RELATED PROCEEDINGS APPENDIX:

None.